X_CAN IP-Module Overview

Robert Bosch GmbH, ME-IC/PRM-IP, 3rd June 2024

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CAN XL – Next Step in CAN Evolution

Superior up to 20 Mbit/s network solution

IP available

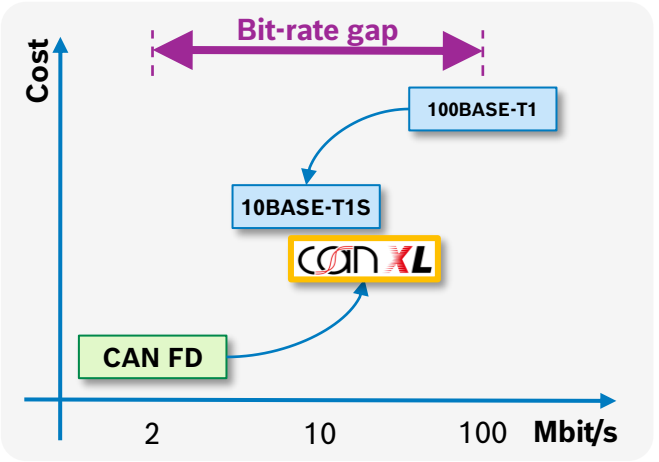
Broad availability in nextGen µCs

Target / Motivation

Provide a superior ≤20Mbit/s CAN solution with respect to

- Price (Transceiver, Pins, Cabling, ...)
- Safety and Security
- Enables SOA (Service Oriented Architecture)
- Quality of Service

Preserve CAN properties: Arbitration, robustness, long stubs, ...



Compatibility of CAN FD and XL enables ...

- Incremental upgrade path
  ➔ larger acceptance (re-use of CAN / CAN FD knowhow and equipment)
- E/E Architecture design freedom: "mixed FD/XL" or "XL only" networks:
  - "XL only" networks up to 20 Mbit/s
  - "mixed" networks limited to 8 Mbit/s (e.g. XL 8 Mbit/s, FD 2 Mbit/s)

Key Success Factors

1) **Cost Optimal E/E Architectures**
   Single bus for 3 types of traffic
   (CAN FD, CAN XL and Ethernet)
2) **Bit rate up to 20 Mbit/s**
   Compatible with wide range of transc.
   (HS-CAN, FD, SIC, SIC XL)
3) **Large payload size (1 .. 2048 bytes)**
   enough space for any application
4) **Ethernet Tunneling**
   allows use of TCP/IP, SOME/IP, etc.
5) **Incremental upgrade**
   Allows CAN FD and CAN XL on the same network (up to 8 Mbit/s)
6) **Scalable**
   flexible tradeoff between cost, speed and network complexity
7) **Broad availability**
   majority of nextGen automotive µCs

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X_CAN Overview

FEATURES

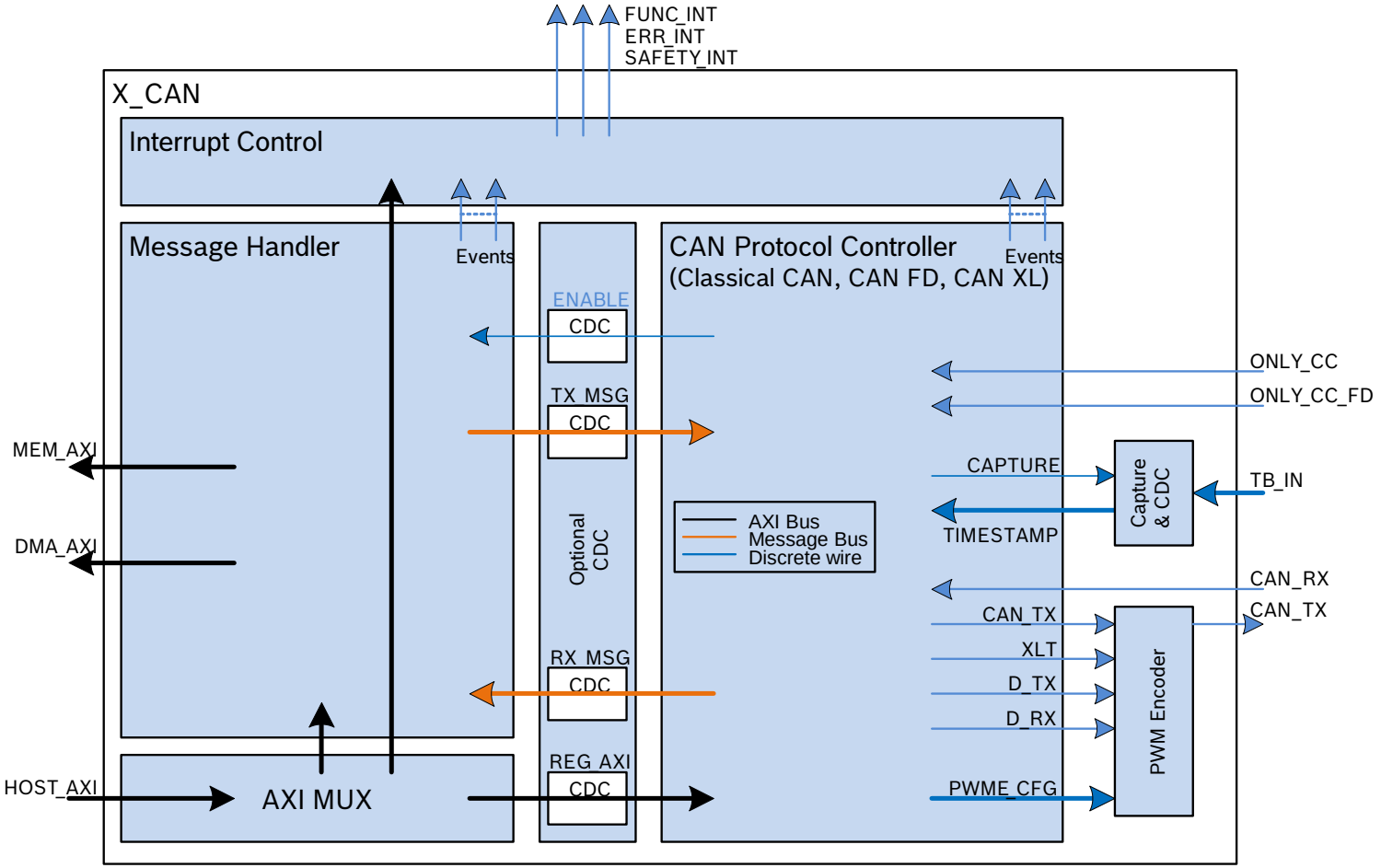
- Support of CAN CC, CAN FD, and CAN XL
  - Conform with ISO11898-1:2024
- Full support of CAN XL protocol
  - Up to 20Mbit/s and up to 2048 bytes
- Small local memory
  - approx. 4 Kbytes for up to 255 filter elements
- Internal DMA engine, XCAN acts as DMA master for message handling
  - Message storage in system memory
  - Low CPU impact, any accesses to/from the system memory are done using the internal DMA engine (less interrupts)
- 8 RX FIFO queues, each with up to 1024 messages
- 8 TX FIFO queues, each with up to 1024 messages
- 1 TX priority queue, up to 32 slots, configurable by SW
- 255 RX filters on the first 8 byte of a frame (e.g., CAN XL header and AF)
- TX filtering capabilities to support security
- Privileged accesses to protect configuration and RX/TX filtering (optional)
- 64-bit Timestamps from external Timebase
- ASIL D capable with external measures

X_CAN Overview

FEATURES

- AXI interface compliant to AMBA 4 ARM Ltd protocol
  - AXI4-Lite slave interface (HOST_AXI)
  - AXI4 master DMA interface (DMA_AXI)
  - AXI4 master Local Memory interface (MEM_AXI)
- CAN Error Logging
- Fault Injection Module
- Programmable loop-back test mode
- Multiple X_CAN can share the same Local Memory
- Maskable module interrupts with three categories: Functional, Functional Error and Safety
- Three clock domains (HOST, CAN, TIMEBASE)
- Power-down support

X_CAN Overview
Block diagram (simplified)



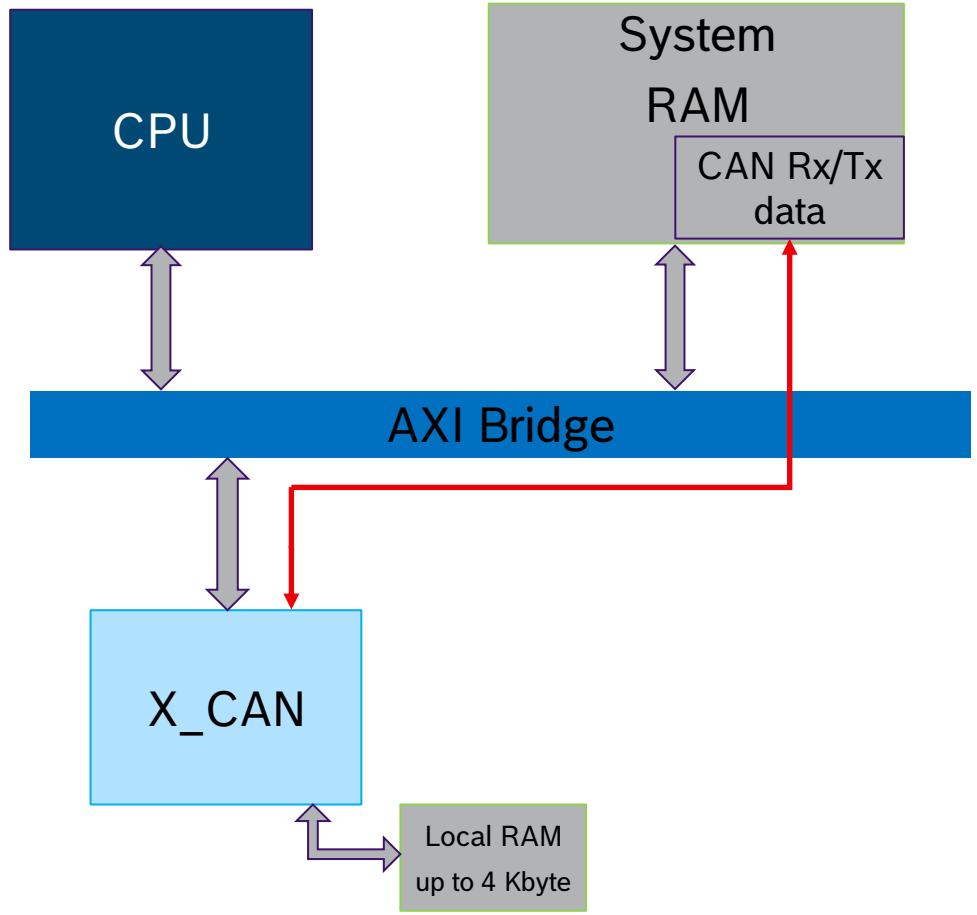
Signal	Dir	Function
HOST_AXI	I/O	RD/WR access to config/control/status registers
DMA_AXI	I/O	DMA Interface for message transfer between XCAN and System RAM
MEM_AXI	I/O	Interface to local Message RAM
FUNC_INT	O	Functional Interrupt
ERR_INT	O	Error Interrupt
SAFETY_INT	O	Safety Interrupt
CAN_RX	I	CAN receive input from transceiver
CAN_TX	O	CAN transmit output to transceiver
TB_IN	I	Time Base Input from external counter for 64-bit time stamping
ONLY_CC_FD	I	If fixed to '1' only Classical CAN and CAN FD operation enabled
ONLY_CC	I	If fixed to '1' only Classical CAN operation enabled

Glossary:

- CDC - Clock Domain Crossing

X_CAN Overview
X_CAN is DMA Master

- Advantages
  - RX/TX data stored in system memory
    - All data handled in system memory
    - No extra transfers from/to local RAM to be initiated by CPU
    - Reduced interrupt load for processor core
  - Only small local RAM required (up to 4 Kbyte)
    - Local RAM buffers part of RX/TX messages during transfer from/to system memory
    - Local RAM holds acceptance filter elements
    - Local RAM holds active descriptors for DMA transfer to system memory



X_CAN Overview
Timeline & Deliverables

Revision 1.1.0
Available

Deliverables include:

- VHDL Source Code
- User Manual (programmer's view)
- Module Integration Guide (designer's view)
- FMEDA
- Safety Manual
- Functional Safety assessment certificate
- Conformance Test Report for CAN and CAN FD
  - Passed in June 2022

Licensing conditions available at Bosch AE
Please see: https://www.bosch-semiconductors.com/ip-modules/can-protocol-license/

Revision 1.1.0
CAN XL Conformance tested
depending on availability of CAN XL CT

Planned for Q1/2025

Conformance Tested for Classical CAN, CAN FD, and CAN XL