Bosch IP TechDay 2024

GTM Technical Overview

ME-IC/PRM-IP | March 15th, 2024

IP TechDay
We enable possibilities

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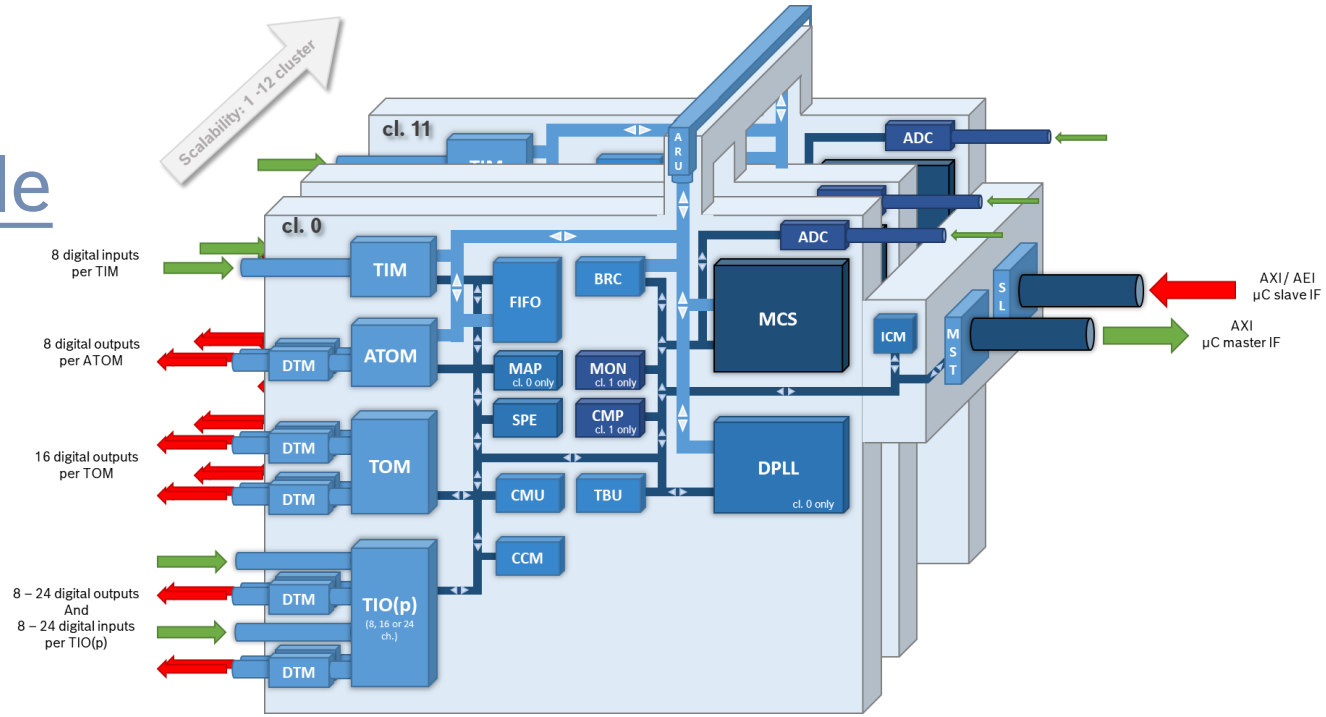
GTM-IP
Agenda

1. What is the GTM?
2. Infrastructure Module
3. I/O Modules
4. Special Function Module
5. Safety Module
6. Core Module



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1

GTM Introduction

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GTM-IP – Architecture
What is GTM (Generic Timer Module)?

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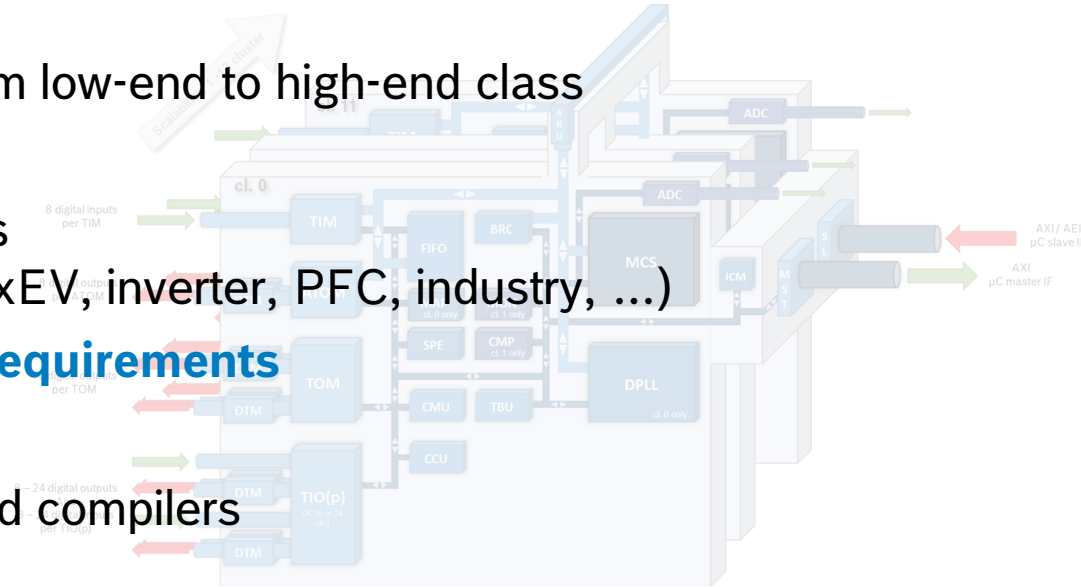
- **Offloading real-time critical I/O workloads from µC cores to a specialized I/O co-processor with massive parallel thread handling capabilities**
- **Common architecture across multiple semiconductors**
  - Development of software/applications independent of selected MCU
- **Scalable design approach**
  - Scales with the application demand – from low-end to high-end class
- **Generic architecture**
  - Covering a wide range of application domains (powertrain, traction control, chassis control, xEV, inverter, PFC, industry, …)
- **Open to 3rd parties to contribute to nextGen requirements**
- **Growing Eco-Environment**
  - Enables development of a rich set of tools and compilers



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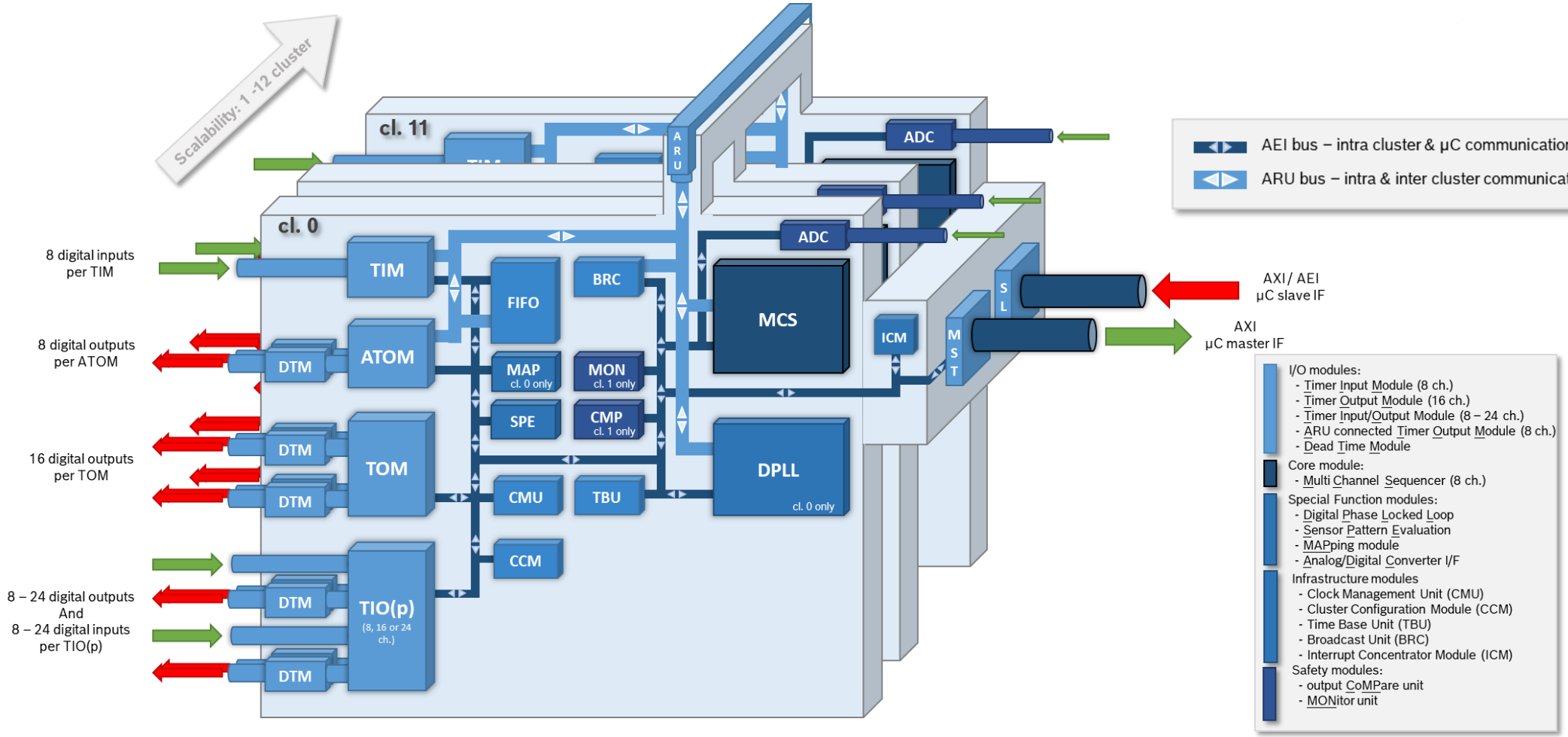
GTM-IP – Architecture
Overview GTM



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GTM
Infrastructure Modules

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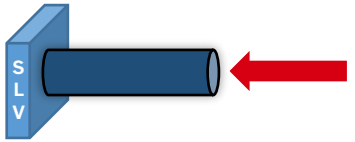
GTM-IP – Architecture
µC to GTM interface [AEI or AXI slave]



µC to GTM interface [AEI or AXI slave]
Primary access path from µC bus masters (usually µC cores) to GTM resources

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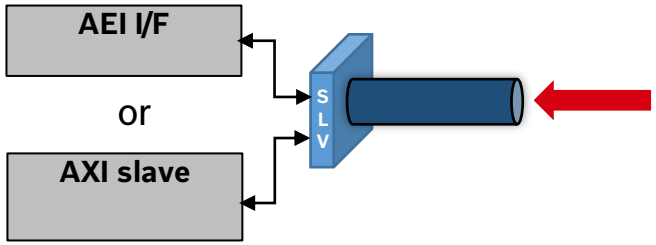
- The GTM−IP is equipped with 2 slave Interfaces
  - a generic bus interface AE Interface (AEI)
  - a AXI slave, Full AMBA AXI 3.0 compliant)
- Via the slave I/F all modules in the GTM can be controlled/configured in each cluster



Note:
Only one of the two µC slave interfaces is available depending to device configuration.

AEI = Automotive Electronics Interface
AXI = Advanced eXtensible Interface

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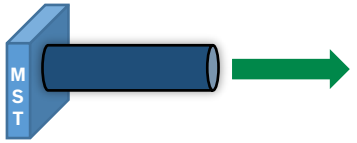
GTM-IP – Architecture
GTM to µC interface [AXI master]



GTM to µC interface [AXI master]

GTM bus master interfaces; enables MCS to access/control µC resources outside GTM

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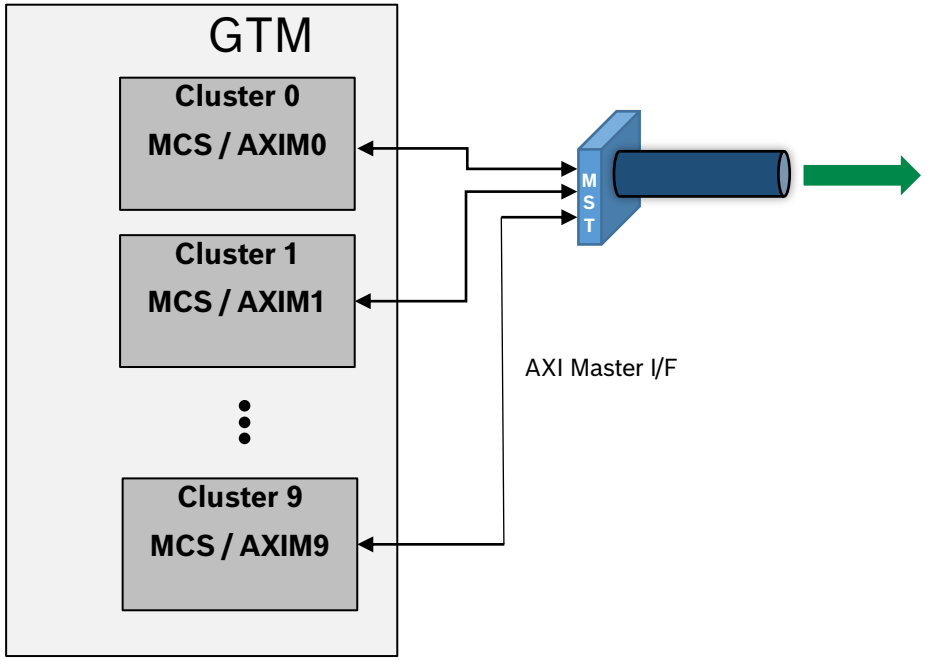
- AXI master (Full AMBA AXI 3.0 compliant)
  - the GTM MCS
  - Max 10 MCS / AXI master
- The MCS (Multi Channel Sequencer) Core can control via the AXI master peripherals/memory on the Soc
  - Depending on the implementation by the integrator



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GTM-IP – Architecture
CMU - Clock Management Unit

CMU
cl. 0 only

Clock Management Unit
Infrastructure module and GTM configuration management

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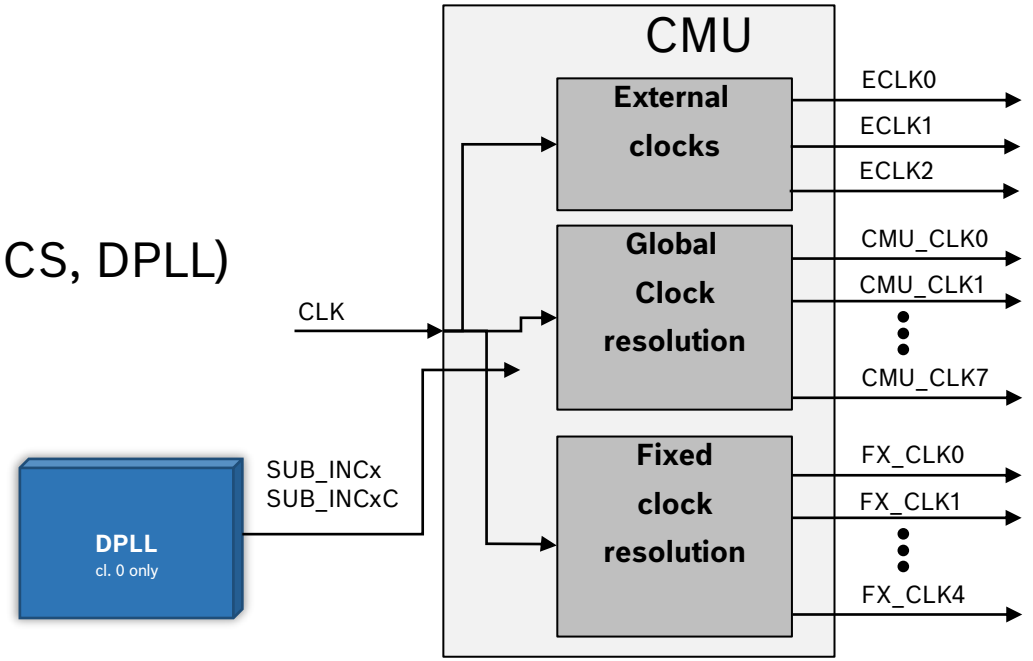
- The Clock Management Unit (CMU) enables/generated the 14 clock sources of the GTM
  - External clock
    - External of GTM
  - Clock resolution (Timer resolution)
    - Global (TIM, ATOM, TBU, TIO,DTM, MCS, DPLL)
      - SW conf dividers
    - Fixed (TOM only)
      - 5 fixed dividers



- The CMU is only available in cluster 0.

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GTM-IP – Architecture
TBU - Time Base Unit

Time Base Unit
Multi-channel timebase unit. Provides multiple timebases for GTM resources

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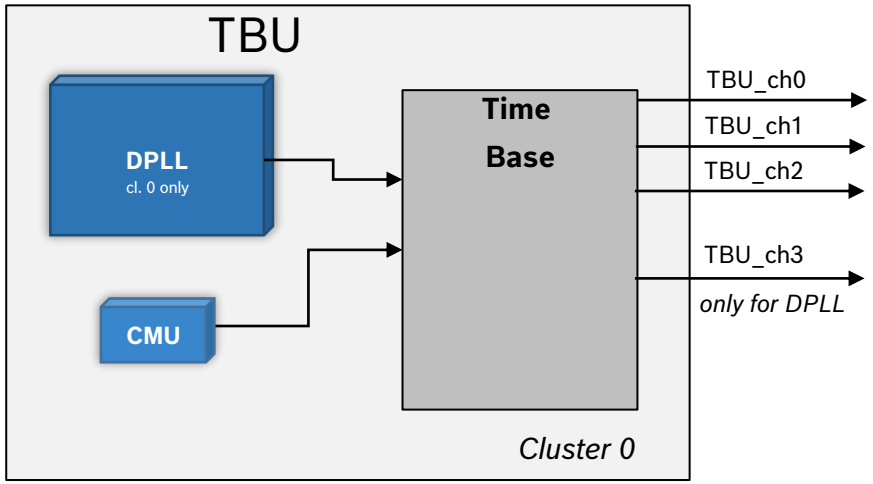
- The Time Base Unit TBU provides common time bases for the GTM−IP.
  - Organized in channels
    - number of channels is device dependent
    - up to four channels



- There are 3 modes:
  - Free Running Counter Mode
  - Forward/Backward Counter Mode
  - Modulo Counter Mode

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GTM-IP – Architecture
CCM - Cluster Configuration Module

CCM

Cluster Configuration Module

Cluster Infrastructure module and configuration management

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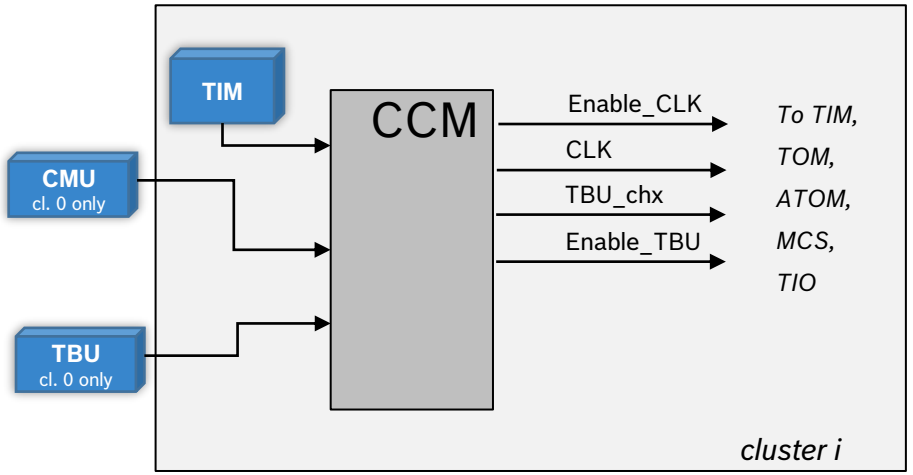
- The Cluster Configuration Module (CCM) enables the configuration of several cluster specific options namely:
  - cluster's clock frequency
  - module clock gating
  - status observation of the cluster's MCS bus master (AEM),
  - address range protection
  - global architecture configuration
  - TIM input as clock resolution



Only showed the CCM clk and gating functions

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GTM-IP – Architecture

AEI Bus inside each cluster

Intra cluster communication

AEI (AE Interface) Bus

GTM communication path inside a cluster for all modules from the slave AXI/AEI I/F

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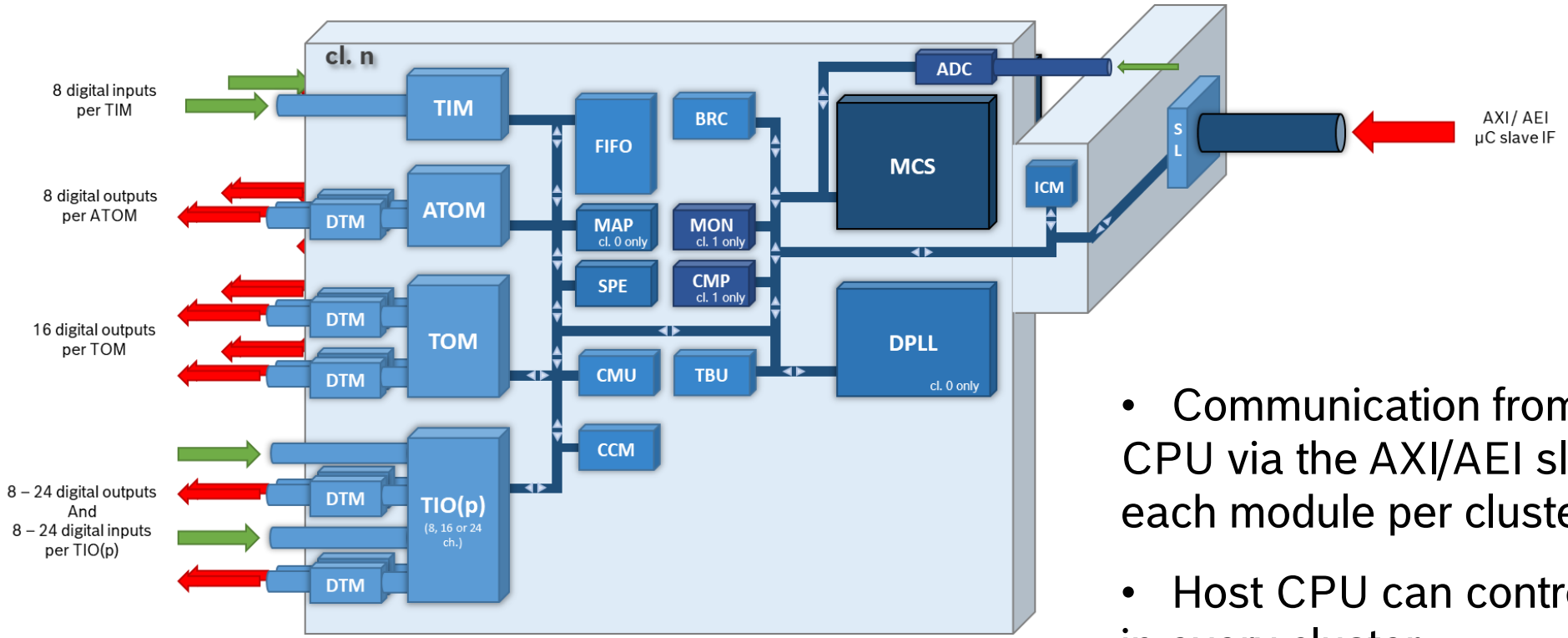

- Communication from the Host CPU via the AXI/AEI slave I/F to each module per cluster
- Host CPU can control all modules in every cluster

Only AEI bus shown in one cluster

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GTM-IP – Architecture

ARU - Advanced Routing Unit
Intra and Inter cluster communication

Advanced Routing Unit
GTM communication path for ARU-connected modules. Intra- and inter-cluster communication

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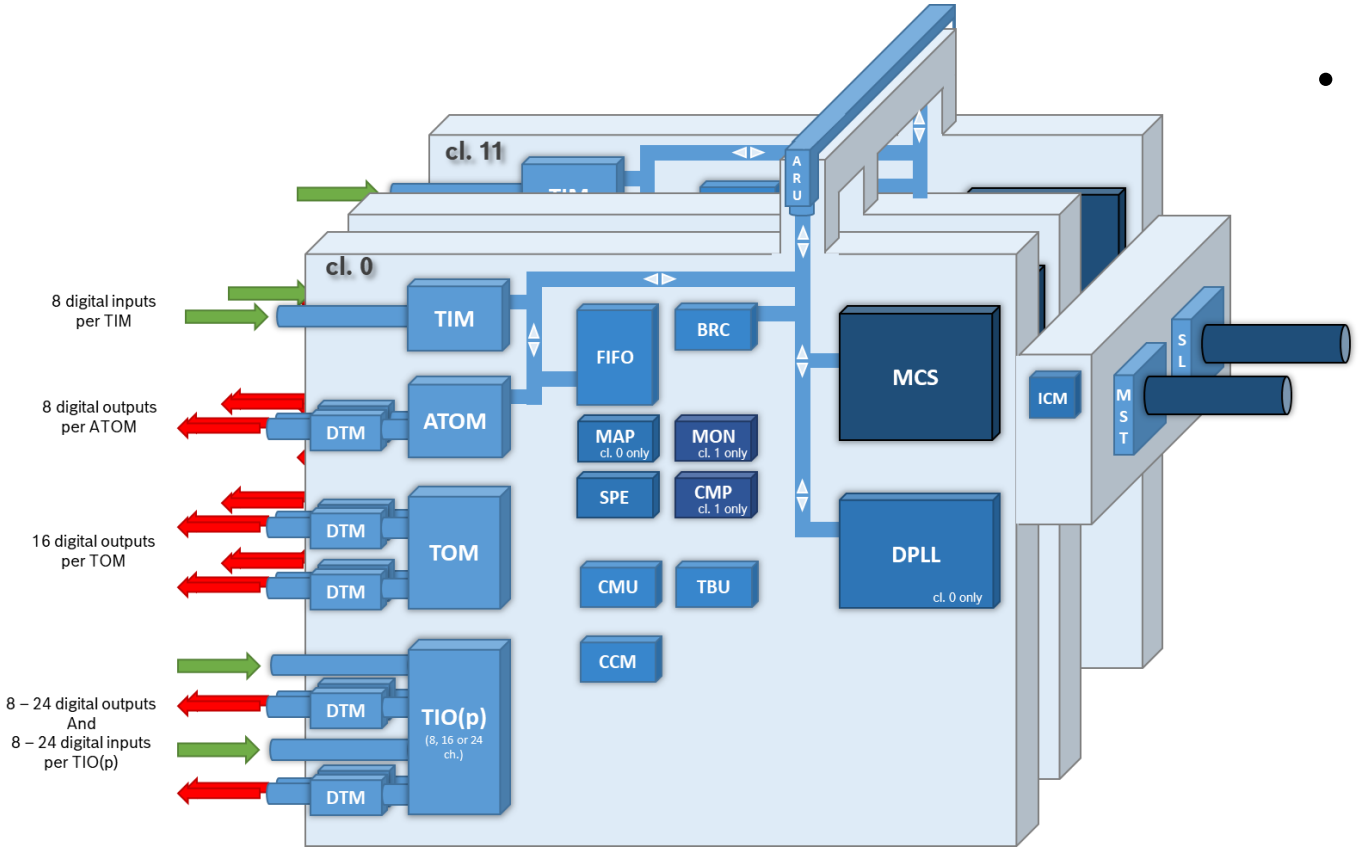

Only ARU bus shown

- The Advanced Routing Unit offers:
  - Intra cluster communication
  - Inter cluster communication
  - For the TIM / ATOM / BRC / DPLL / MCS and FIFO

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GTM-IP – Architecture
ARU - Advanced Routing Unit

Advanced Routing Unit
GTM communication path for ARU-connected modules. Intra- and inter-cluster communication

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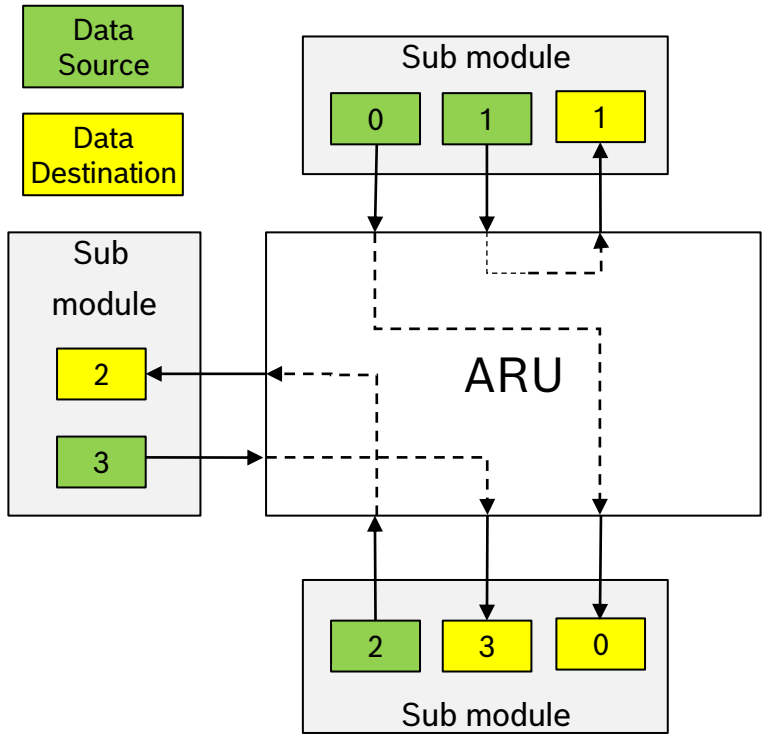
- The ARU (Advanced Routing Unit) provides a flexible and resource efficient way for connecting any data source to an arbitrary data destination inside the GTM
  - Intra cluster communication
  - Inter cluster communication
- P2P (Point to Point) connection



ARU data routing principle.

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GTM-IP – Architecture
BRC - BRoadCast Unit

BRoadCast Unit
ARU broadcast communication support

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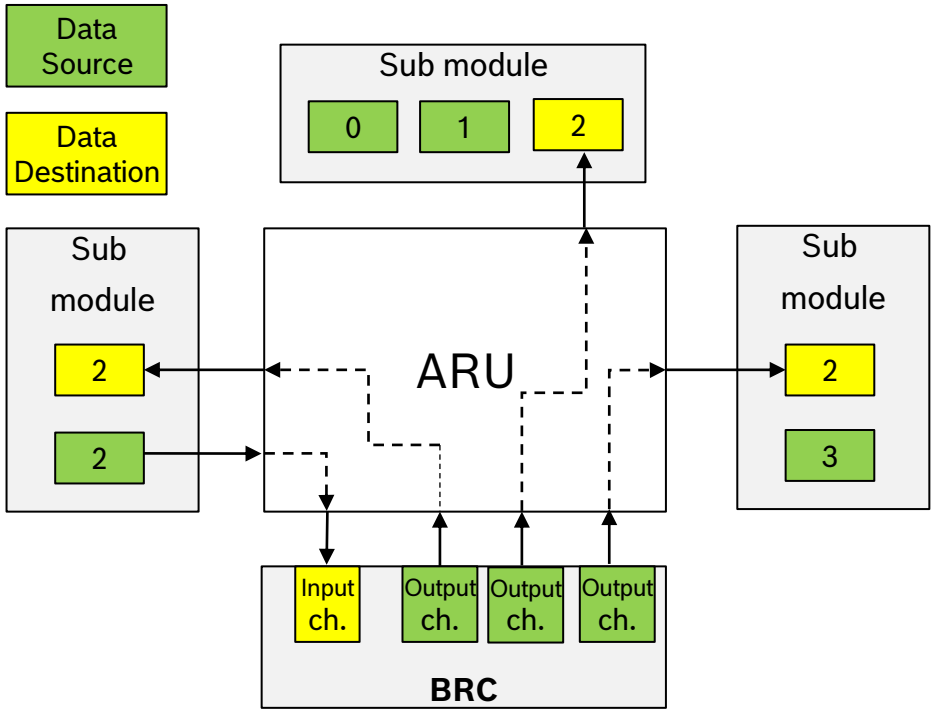
- The Broadcast (BRC) enables duplication of data streams (output of modules) to multiple destination (different input channel of modules)
  - The BRC submodule provides 12 input channels as well as 22 output channels.



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GTM-IP – Architecture
FIFO – First In First Out Unit

FIFO Unit
ARU connected FIFO memory

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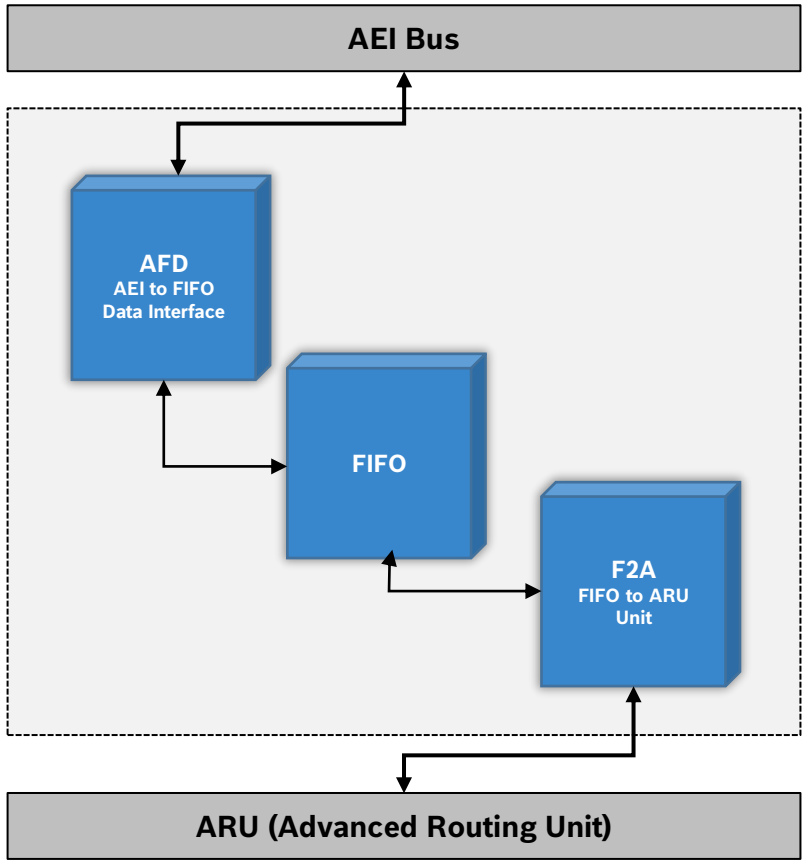
- Application usage:
  - store data in the GTM and send data out of the GTM.
  - F2A (FIFO to ARU unit)
    - Interface of the FIFO to the ARU bus
  - AFD (AEI to FIFO Data Interface)
    - interface of the FIFO to the AEI bus.



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3

GTM 4.1
I/O Modules

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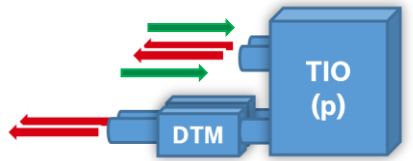
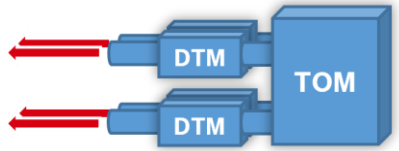
GTM-IP – Architecture
Overview – Timer Units

- TIO – Timer Input Output Module
  - Low-complexity Timer for PWM, filtering and serial shift
- TIM – Timer Input Modules
  - Filtering and capturing of input signals e.g.
    - Timeout Detection / Input Edge Counter
    - Signal Measurement (PWM duration)
- TOM – Timer Output module
  - Generate PWM Signals
- ATOM – ARU connected TOM
  - Able to generate complex waveforms
- Dead Time:
  - Change of output signal



Timer Input Output Module
8 to 24 I/O channels
w/ capture incl. basic input filters)
(p) = plus (increment/decrement/compare/shift)

Timer Input Module
8 channels of complex capture & compare functions (incl. input filters)



Timer Output Module
16 channels of complex output waveform generation (PWMs)

ARU connected Timer Output Module
8 channel advanced TOM functionality

Dead Time Module
Support for delayed, inverted or duplicated output signals including cross-channel combinatorial post-processing of output signals

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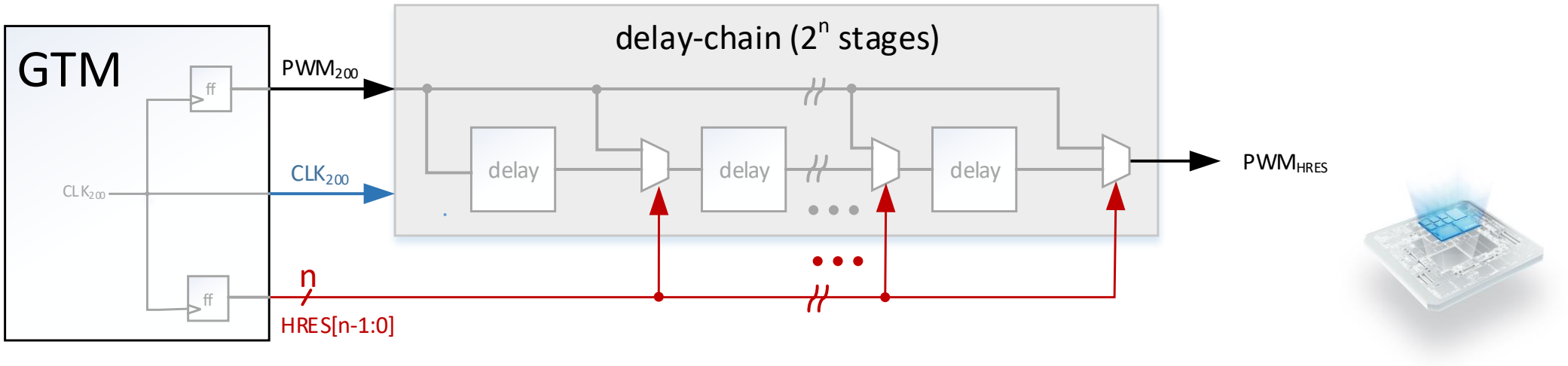
GTM-IP – Architecture
HighRes

- Support for HighRes PWM generation
  - Generating PWM at resolutions up to 156.2 ps (GTM @ 200 MHz; n = 5) with external delay chain solution



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GTM
Special Function modules

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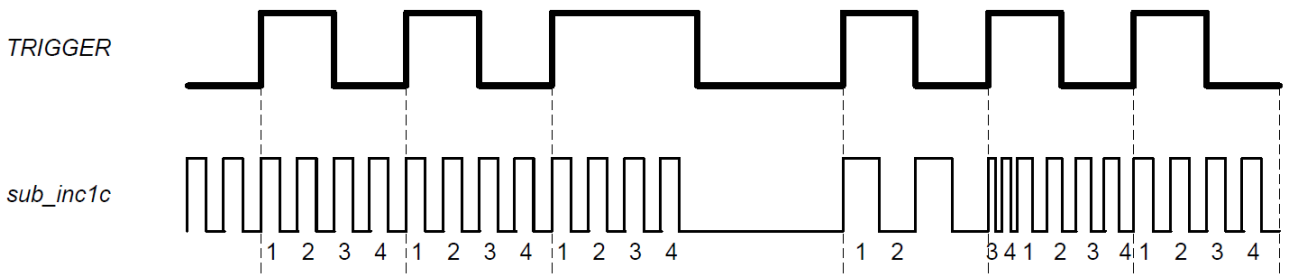
GTM-IP – Architecture
DPLL
Digital Phase Locked Loop

Digital Phase Locked Loop
Engine positioning management including high resolution angle clock base and dynamic scheduling of trigger events

- The digital PLL Phase Locked Loop (DPLL) submodule is used for frequency multiplication.
- Application Usage:
  - Calculation of the position information of linear or angular motions, mass flow values, temperature, pressure or level of liquids, for example engine positioning detection and signaling (angle clock).

- Example for four times higher frequency:
  - DPPL is configured to generate 4 micro ticks [sub_inc1c (output of DPLL)] per tick from Trigger (input of DPLL) (Tick is from rising edge to rising edge)



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GTM-IP – Architecture
MAP - MAPing module

MAP
cl. 0 only

MAPing module
Input channel mapping unit

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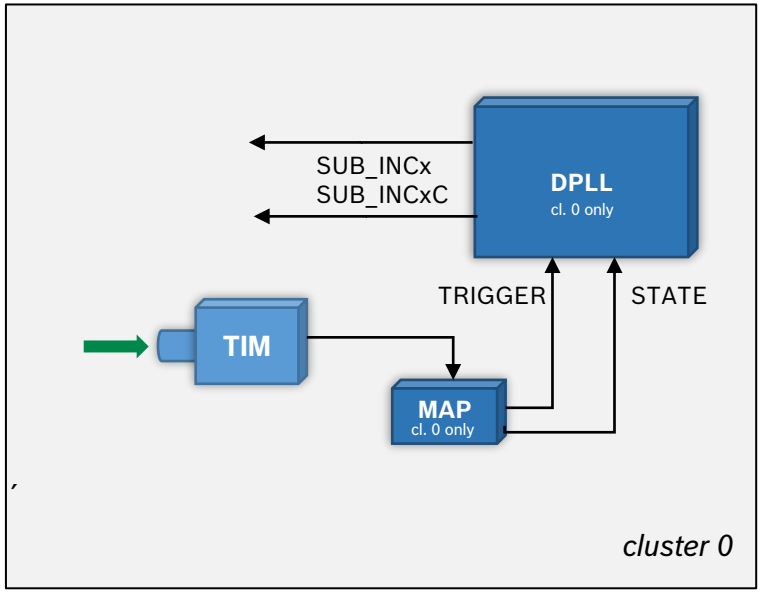
- The MAP Mapping submodule generates the two input signals TRIGGER and STATE for the submodule DPLL by evaluating the output signals of the channel 0 up to channel 5 of submodule TIM0 (only cluster 0).

- By using the TIM as input submodule, the filtering of the input signals can be done inside the TIM channels themselves.



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GTM-IP – Architecture
SPE – Sensor Pattern Evaluation Unit

SPE

Sensor Pattern Evaluation Unit
Evaluation of incoming sensor data pattern

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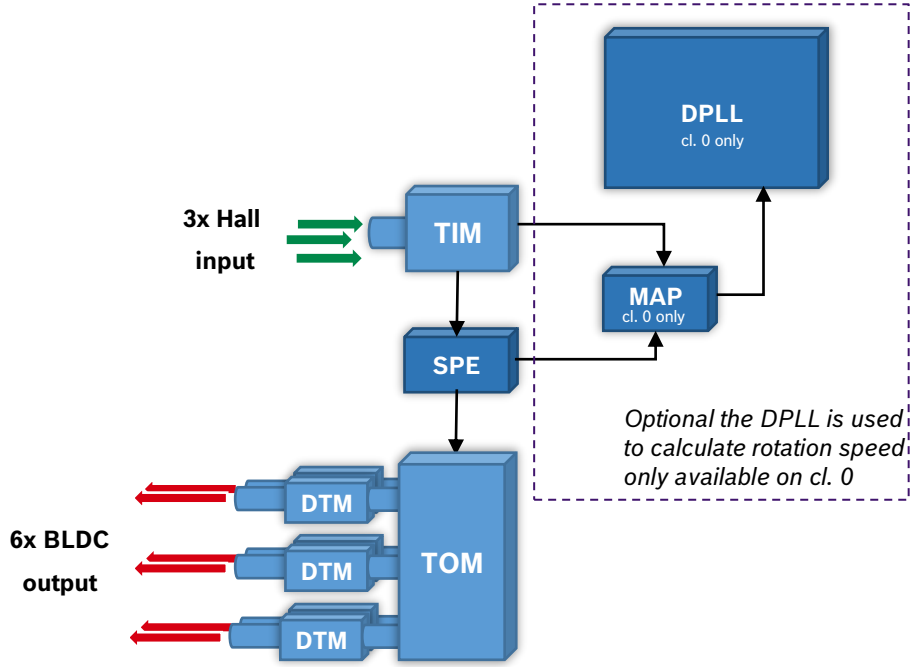
- The Sensor Pattern Evaluation (SPE) submodule can be used to evaluate three hall sensor inputs and together with the TOM module to support the drive of BLDC (Brush-Less DC) motors.

- Input signals are filtered already in the connected TIM channels.



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GTM
Safety modules

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GTM-IP – Architecture
CMP - CoMPare Unit

CMP
cl. 1 only

CoMPare Unit
Signal compare unit

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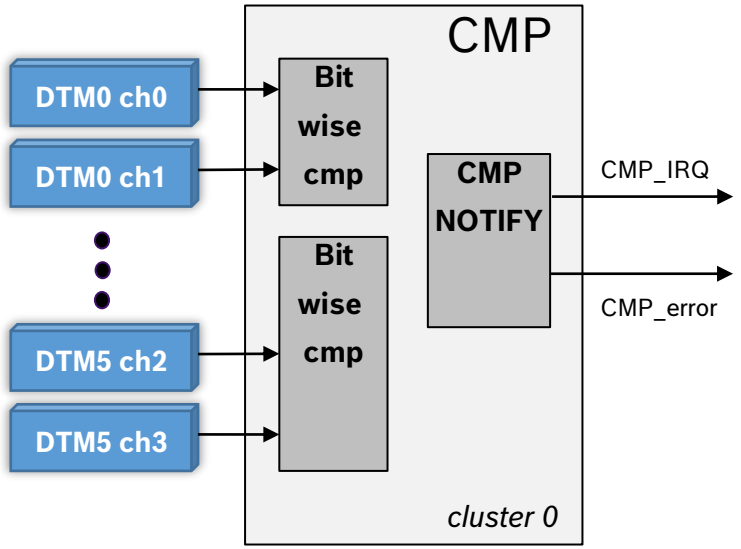
- Application usage:
  - Comparing duplicate outputs
    - The CMP submodule can compare two adjacent channel outputs from TOM or ATOM submodules and raises an error, when the two signals are not identical.
      - max 2x24 ch



Example Application
Input to DTM are TIM/TOM/TIO

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GTM-IP – Architecture
MON - MONitor Unit

MON
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MONitor Unit
Signal monitoring unit

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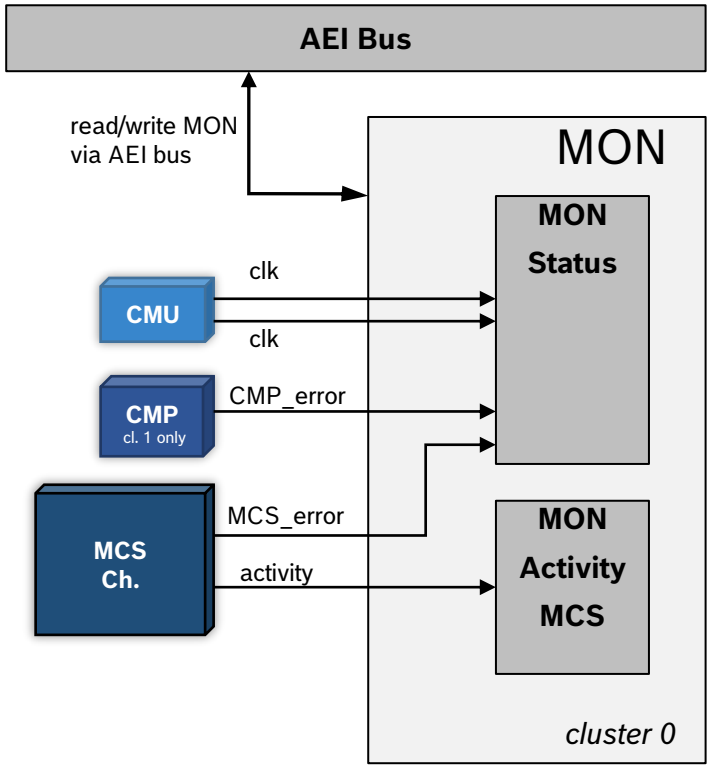
- The MON submodule monitors the GTM internal clocks and the MCS functionality.
  - the activity of the clocks is supervised
    - No activity leads to Safety INT
  - Characteristics of signals can be checked in MCS
  - the ARU cycle time can be compared in a MCS channel to given values



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GTM
Core module

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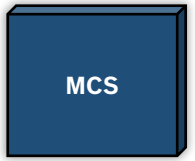
GTM-IP – Architecture
MCS - Multi Channel Sequencer



Multi Channel Sequencer
real-time optimized RISC cores with
8 parallel threads

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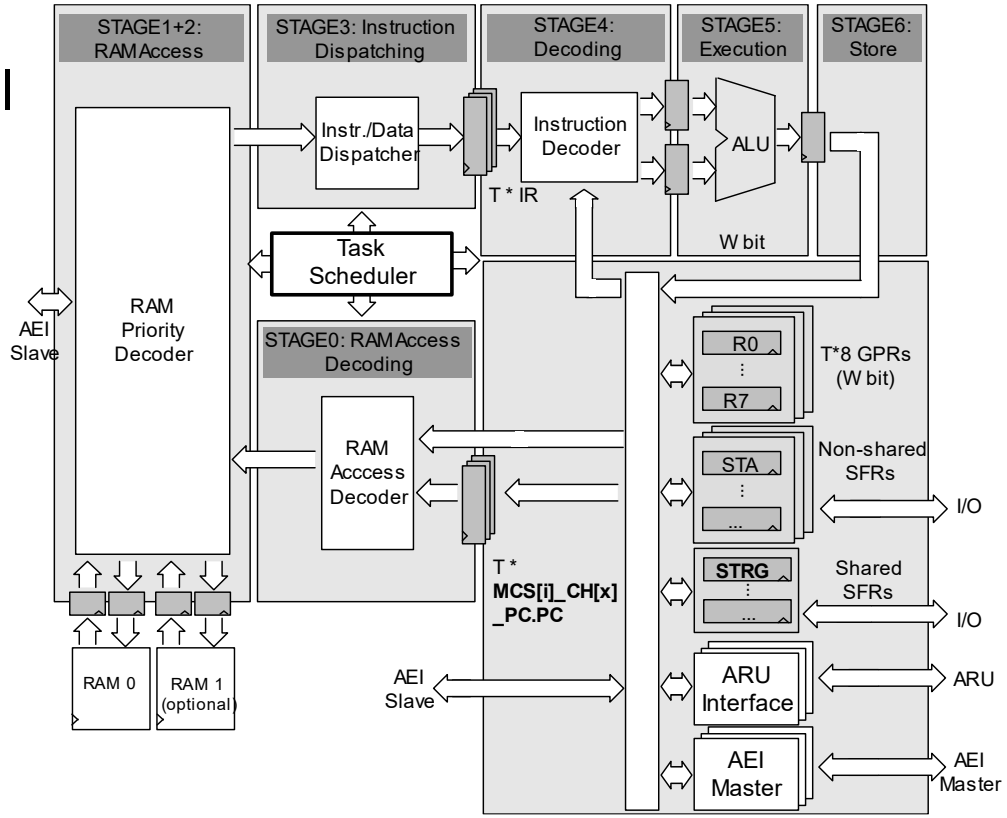
- The MCS is a 24bit instruction RISC (Reduced Instruction Set Compute) CPU core with 8 parallel threads
  - Determistic, every 9th cycle 1 thread is executed
  - Control/monitor internal GTM signals and external modules on the Soc/µC
- Master for all modules in a cluster
  - MCS has priority over slave I/F AEI or AXI
  - Every 9th cycle is reserved for slave I/F AEI or AXI
  - MCS can be stopped for bus access
- ARU connection to other cluster.



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GTM-IP – Architecture
MCS - Multi Channel Sequencer

Multi Channel Sequencer
real-time optimized RISC cores with 8 parallel threads

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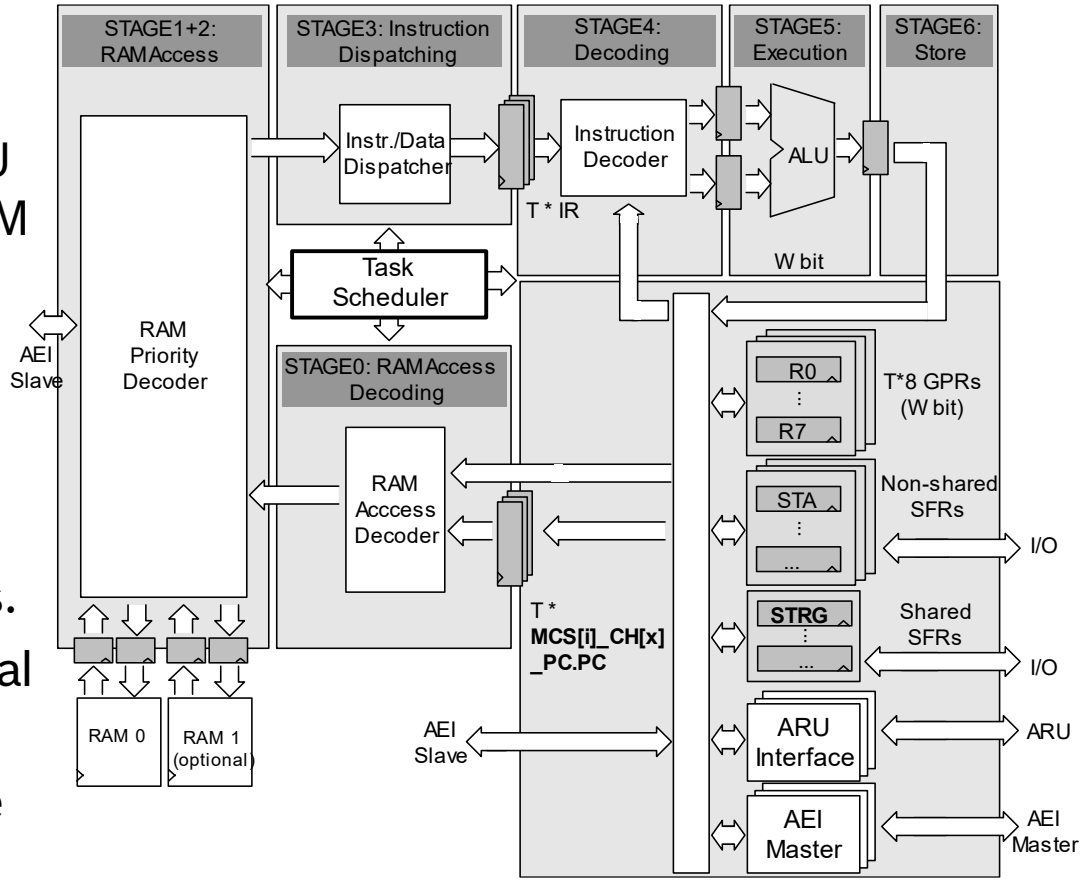
- Application usage:
  - is to calculate complex output sequences that may depend on the time base values of the TBU and are processed in combination with the ATOM submodule
  - to perform extended data processing of input data resulting, e.g. from the TIM submodule
  - process data provided by the CPU within the MCS submodule, and the calculated results are sent to the outputs using the ATOM submodules.
  - E.g. thread waits for condition of an SFR (Special Function register) or time base value
    - SFR can change with an INT from a module (e.g. TIM)



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Thank you!

Juergen Hanisch
Gregor Sunderdiek

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